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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	09/460,742	NAIR ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,14-16 and 29-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,14-16 and 29-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 12/27/04. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Chern et al. (USP 6448628).

As to claim 14, Chern et al.'s abstract and figure 9 show a circuit comprising a die (circuit figure 9 is integrated circuit); a ground node (VSS) located on the die; power supply voltage node (Vcc); and an electronic device (figure 9) having a variable capacitance characteristic (figure 9 is a depletion mode capacitor, which, by nature, is a variable capacitor) and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical to incremental voltage variations about an operational node voltage at the power supply voltage node (both of Applicant's capacitor and Chern et al.'s capacitor area depletion mode. Therefore, they have similar operation characteristic).

As to claim 15, since electric property of Applicant's capacitor is similar to Charn et al.'s capacitor, the accompanying characteristics including the damping and amplifying are inherent.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-6, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizaki et al. (USP 6384674) in view of Manning et al. (USP 5962887).

As to claim 4 and, Tanizaki et al.'s figure 2 shows a circuit comprising: a voltage node (VP); a ground node (VSS); and a capacitor (VSC) connected between the voltage node and ground node. Tanizaki fails to teach that the capacitor is transistor connected capacitor. However, Manning et al.'s figure 1 shows a capacitor connected transistor including gate comprising p-type polysilicon (column 1, lines 52-58); a gate oxide layer (capacitor figure 1 is metal-oxide-semiconductor. Therefore, the dielectric layer 110 is oxide layer), a drain (130 or 140), and a source (140 or 130), the transistor to operate in the depletion mode (depending on the value of voltage 160, figure 2 shows transistor 2 is operating in depletion mode for certain of range). The capacitor connected transistor of Manning et al. has the advantage of increasing voltage range. Therefore, it would have been obvious to one having ordinary skill in the art to use Manning et al.'s capacitor connected transistor for Tanizaki et al.'s capacitor VSC and also for capacitors SC and VDC for the purpose of increasing the voltage range. Thus, the modified Tanizaki et al.'s figure 2 shows all limitations of the claim except for the gate oxide layer having thickness of between 20 angstroms and about 40 angstroms. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by

routine experimentation and optimization to choose the particular claimed relative thickness limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative thickness. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the thickness of

Manning et al.'s layer 110 to be between 20 angstroms and about 40 angstroms dependent upon particular environment of use to ensure optimum performance.

As to claim 14, the modified Tanizaki et al.'s figure 2 shows a circuit comprising a die (circuit figure 2 is integrated circuit), a ground node (VSS) located on the die; power supply voltage node (VP); and an electronic device (the modified VSC) having a variable capacitance characteristic (Manning et al.'s figure 2) and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical to incremental voltage variations about an operational node voltage at the power supply voltage node (the modified Mnnning's transistor having similar structure with Applicant's transistor. Therefore, Manning et al.'s transistor is capable of perform similar function as Applicant's transistor).

As to claim 15, since electric property of the capacitor as shown in the modified Tanizaki et al.'s figure 2 is the same as the claimed capacitor transistor whose property is shown in figure 1B of the application and the prior art discloses all the claimed structure, the accompanying characteristics including the damping and amplifying are inherent.

As to claims 5 and 16, the modified Tanizaki et al.'s figure 2 shows all limitations of the claims except for the voltage of at the node between VP and ground is between about 0.5 volts and about 1.5 volts or at 1.3 volts. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative operating voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would

possess utility using another relative operating voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the operating voltage for Tanizaki et al.'s capacitor to be between about 0.5 volts and about 1.5 volts or at 1.3 volts (by selecting certain value of Vcc) dependent upon particular environment of use to ensure optimum performance.

As to claim 6, the modified Tanizaki et al.'s figure 2 further shows a logic cell (106) coupled to the voltage node and close to the transistor.

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizaki et al. (USP 6384674) in view of Manning et al. (USP 5962887) and Yoneda et al. (USP 4906594).

The combination of Tanizaki et al. and Manning et al. references (see the rejection of claim 4) teaches all elements of the claim except for the transistor formed on a silicon-on-sapphire (SOS) substrate. However, Yoneda et al. teaches in column 1, lines 35-40, that SOS substrate has excellent characteristics such as higher speed owing to decreased floating capacity. Thereby improving the operation characteristics for the integrated circuit. Therefore, it would have been obvious to one having ordinary skill in the art to use silicon-on-sapphire as a substrate of Tanizaki et al's transistor for the purpose of improving the operation characteristic for the transistor.

6. Claims 30 ad 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizaki et al. (USP 6384674) in view of Manning et al. (USP 5962887) and Yoneda et al. (USP 4906594) and Jones et al. (USP 5632855).

As to claim 30, the combination of Tanizaki et al., Manning et al. Yoneda et al. references shows all limitations of the claim except for the oxide layer comprises a thermal oxide. However, Jones et al. teaches in column 1, lines 10-13, that thermal oxidation is the most viable way to form an oxide. Thermal oxide serves numerous purposes, such as preventing formation of certain types of thin films upon the oxide while allowing those types of films to form in area void of oxide. Thus, it would have been obvious to one having ordinary skill in the art to form the oxide layer by thermal oxidation process for the purpose of preventing formation

of certain types of thin films upon the oxide while allowing those types of films to form in area void of oxide.

As to claim 31, the modified Tanizaki et al's figure 2 further shows a logic cell (106) coupled to the voltage node and close to the transistor.

7. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizaki et al. (USP 6384674) in view of Manning et al. (USP 5962887) in view of Abrokwah et al. (USP 5539248).

As to claims 32 and 33, the combination of Tanizaki et al. and Manning et al. references (see the rejection of claim 4) teaches all elements of the claim except for gallium arsenide die. However, Abrokwah et al. teaches column 1, lines 15-16, that gallium arsenide devices have an advantage over silicon device in speed and power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use gallium arsenide as the substrate for Tanizaki et al. circuit for the purpose of improving speed and power consumption.

As to claim 33, the modified Tanizaki et al.'s figure 2 shows the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and drain are coupled to the low power supply voltage node.

As to claim 34, the combination of Tanizaki et al. and Manning et al. and Abrokwah et al. references shows all limitations of the claim except for the gate oxide layer having thickness of between about 20 angstroms ad about 40 angstroms. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative thickness limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose,

produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative thickness. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the thickness of Manning et al.'s layer 110 to be between 20 angstroms and about 40 angstroms dependent upon particular environment of use to ensure optimum performance.

8. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizaki et al. (USP 6384674) in view of Manning et al. (USP 5962887) and McKee et al. (USP 6143072).

As to claims 35 and 36, the combination of Tanizaki et al. and Manning et al. references (see the rejection of claims 14 and 15) shows all limitations of the claim except for germanium die. However, McKee et al. teaches in column 1, lines 26-28, that germanium substrate is likely to provide better operating characteristics than those provided by a silicon substrate. Therefore, it would have been obvious to one having ordinary skill in the art to use germanium substrate for Choi''s circuit for the purpose of improving the circuit's operating characteristics.

As to claim 37, the prior arts show all limitations of the claim except for the operational node voltage is about 1.3 volts. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative operating voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative operating voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA

1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the operating voltage for Choi's capacitor to be 1.3 volts (by selecting certain value of Vcc) dependent upon particular environment of use to ensure optimum performance.

Response to Arguments

Applicants' arguments have been fully considered, but they are not persuasive.

Applicants argue that Chern et al. is not a valid 102(e) reference. The Examiner respectfully disagrees. Chern et al.'s reference USP 6448628, is a continuation of US application 07/703235 filed 05/20/91. Thus, the effective filling date of Chern et al.'s reference USP 6448628 is 05/20/91. Therefore, the 102(e) rejection is proper.

In response to the argument regarding to the rejection of claims 4 and 29, the specification at page 6, line 10 states that "A thickness of less than about 20 angstroms may result in manufacturing devices that have low yields, while a thickness of more than about 40

angstroms may result in a device frequency response that is lower than desired." However, the specification in page does not teach the thickness between 20 to 40 angstroms produces an unexpected result. Thus, it is seen as an obvious matter of preference for selecting such relative limitations for Manning et al.'s transistor. Furthermore, it is known that the operation of the circuit is dependent on the gate thickness of the capacitor. One ordinary skill in the art would have motivate to select the gate thickness between 20 to 40 angstroms dependent upon particular environment of use to ensure optimum performance.

In response the argument regarding to the rejection of claims 14-16, Applicants argue that the Office action fails to provide specific, objective evidence of record for a finding of a teaching, suggestion, or motivation to combine reference teaching and fails to explain the reasoning by which the evidence is deemed to support such a finding. The Examiner respectfully disagrees. The motivation to modified Tanizaki et al.'s capacitor is stated in the rejection of claim 4. The modified Tanizaki et al.'s capacitor having similar structure as Applicant's capacitor. Therefore, the modified Tanizaki et al.'s capacitor performs the same function.

In repose to the argument regarding the rejection of claim 31, Tanizaki et al.'s specification teaches that circuit 106 is an inverter (column 13, line 16). It is well known that inverter is a logic circuit. Thus, as broadest as reasonable interpretation, circuit 106 is a logic cell.

In response to the argument of regarding the rejection claim 32, Applicants argue that the Office action fails to address the question of a teaching, suggestion, or motivation, in the record to combine a gallium arsenide die, as taught in Abrokawah et al. with the capacitor of Manning et al. and the circuit shown in Fig. 2 of Tanizaki et al. The Examiner respectfully disagrees.

Abrokwah et al. teaches column 1, lines 15-16, that gallium arsenide devices have an advantage over silicon device in speed and power consumption. Thus, motivation to combine a gallium arsenide die, as taught in Abrokawah et al. with the capacitor of Manning et al. and the circuit shown in Fig. 2 of Tanizaki et al. is improving speed and power consumption.

In response to the argument regarding the rejection of claim 35, McKee et al. teaches in column 1, lines 26-28, that germanium substrate is likely to provide better operating characteristics than those provided by a silicon substrate. Thus, the motivation to combine germanium substrate, as taught by McKee et al. with the capacitor of Manning et al. and the circuit shown in Fig. 2 of Tanizaki et al. is improving the circuit's operating characteristics.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

February 07, 2005